What is claimed is:

1. A semiconductor package comprising:

a semiconductor die having a front side and an opposed backside;

a backside metallization layer formed on the backside of the die;

an integrated heat spreader; and

a thermal interface including a fluxlessly-capable solder portion deposited on a top surface of the integrated heat spreader and bonded to said metallization layer under load and heat.

2. The semiconductor package of claim 1, said backside metallization layer including three layers including an adhesion/barrier layer, a wetting layer, and a protection layer.

3. The semiconductor package of claim 2, said adhesion/barrier layer formed of a material selected from the group consisting of Ti, TiN, Ta, and TaN.

4. The semiconductor package of claim 2, said wetting layer formed of a material selected from the group consisting of NiV and Ni.

5. The semiconductor package of claim 2, said protection layer formed of a material selected from the group consisting of Au, Pt and Pd.

6. The semiconductor package of claim 1, said solder portion including AuSn solder.

7. The semiconductor package of claim 6 wherein said solder portion includes either separate Au and Sn layers or a single eutectic AuSn layer.

8. The semiconductor device of claim 7 wherein a thickness of Au layer and Sn layer is formed so that an overall Au-to-Sn ratio by weight is 80 to 20.

9. The semiconductor package of claim 1, said thermal interface layer including a barrier layer disposed between the solder portion and the integrated heat spreader.

10. The semiconductor package of claim 9 wherein said barrier layer is formed of Ni.

11. The semiconductor package of claim 1, wherein said backside metallization layer includes an adhesion/barrier layer, a wetting layer, and a protection layer, and said thermal interface layer includes a solder portion including gold (Au) and tin (Sn) together with a barrier layer formed of nickel (Ni) disposed between the solder portion and the integrated heat spreader.

12. A method for forming a semiconductor package having a semiconductor die coupled to an integrated heat spreader, the method comprising:

forming a metallization layer on a backside of the semiconductor die;

forming a thermal interface portion on a topside of the integrated heat spreader, said thermal interface portion including a solder layer; and

forcing together under load and heat the metallization layer and the solder layer without flux to bond the semiconductor die to the integrated heat spreader.

13. The method of claim 12, further including heating the package to above 300°C for a package heating time of between about 1 and 30 minutes and ramping down the temperature lower than about 100°C per minute.

14. The method of claim 13, wherein the package heating time is between about 2 and 3 minutes.

15. The method of claim 13, wherein the temperature is ramped down approximately 30°C per minute.

16. The method of claim 12 further including reacting the solder layer with the metallization layer to form bonded intermetallic layers.

17. The method of claim 16, wherein the solder layer includes gold (Au) and tin (Sn) and the metallization layer includes a protection layer formed of a material selected from the group consisting of gold (Au), Platinum (Pt), and Palladium (Pd) and a wetting layer formed of a material selected from the group consisting of nickel-vanadium (NiV) and nickel (Ni).

18. The method of claim 17, wherein the solder layer reacts with the protection layer and wetting layer to form intemetallics using a fluxless bonding approach.

19. The method of claim 18, wherein the solder layer includes gold (Au) and tin (Sn), the protection layer is gold (Au) and the wetting layer is nickel (Ni) where the intermetallic formed is Au-Sn-Ni.

20. The method of claim 12 wherein the metallization layer includes an adhesion/barrier layer, a wetting layer, and a protection layer.

21. The method of claim 12, further including bonding the die of the semiconductor package onto an organic printed circuit board substrate.

22. The method of claim 12 wherein forcing the metallization layer and fluxless solder layer together under load and heat includes placing the package within a reflow oven purged with N_2.

23. The method of claim 12 wherein the step of forcing the metallization layer and fluxless solder layer together under load and heat further includes:

resting the integrated heat spreader on a carrier with the fluxlessly-capable solder layer exposed;

placing the die on top of the integrated heat spreader with the metallization layer in contact with the fluxlessly-capable solder layer;

holding the die onto the integrated heat spreader using a downward force on the package; and

heating the package within a reflow oven purged with N_2.

24. The method of claim 23 wherein the downward force includes a clip holding the die onto the integrated heat.

25. The method of claim 23 further including ramping down the heat applied to the package after heating the package.

26. The method of claim 23 wherein the reflow oven used for heating the package includes multiple zones each with independent temperature controls.

27. The method of claim 26, said reflow oven multiple zones have a maximum temperature of 400°C.